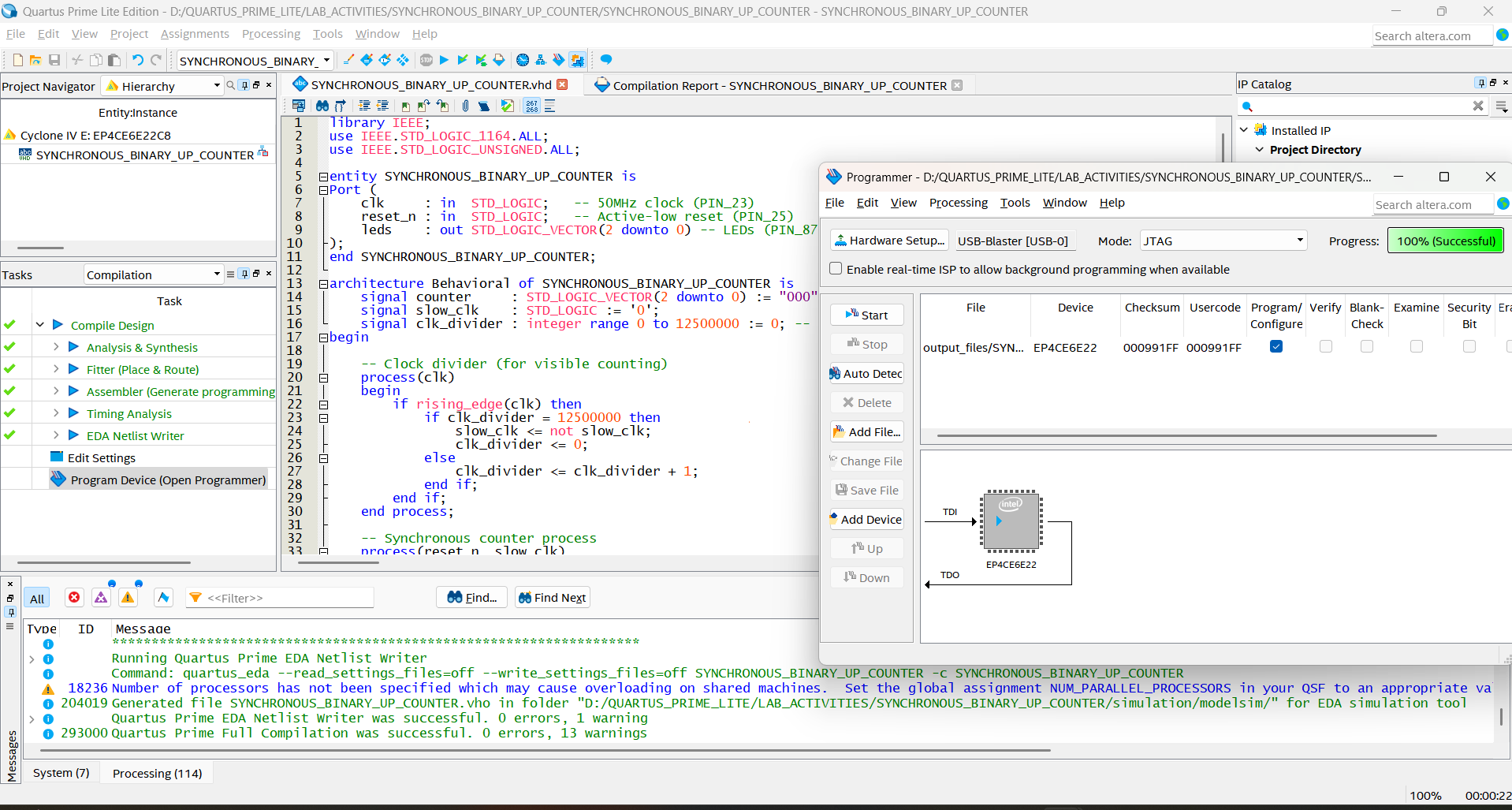
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**SYNCHRONOUS BINARY UP COUNTER**

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

use IEEE.STD\_LOGIC\_UNSIGNED.ALL;

entity SYNCHRONOUS\_BINARY\_UP\_COUNTER is

Port (

clk : in STD\_LOGIC; -- 50MHz clock (PIN\_23)

reset\_n : in STD\_LOGIC; -- Active-low reset (PIN\_25)

leds : out STD\_LOGIC\_VECTOR(2 downto 0) -- LEDs (PIN\_87,86,85)

);

end SYNCHRONOUS\_BINARY\_UP\_COUNTER;

architecture Behavioral of SYNCHRONOUS\_BINARY\_UP\_COUNTER is

signal counter : STD\_LOGIC\_VECTOR(2 downto 0) := "000";

signal slow\_clk : STD\_LOGIC := '0';

signal clk\_divider : integer range 0 to 12500000 := 0; -- 2Hz @ 50MHz

begin

-- Clock divider (for visible counting)

process(clk)

begin

if rising\_edge(clk) then

if clk\_divider = 12500000 then

slow\_clk <= not slow\_clk;

clk\_divider <= 0;

else

clk\_divider <= clk\_divider + 1;

end if;

end if;

end process;

-- Synchronous counter process

process(reset\_n, slow\_clk)

begin

if reset\_n = '0' then -- Active-low reset

counter <= "000";

elsif rising\_edge(slow\_clk) then

counter <= counter + 1; -- All bits update simultaneously

end if;

end process;

-- LED outputs (active-high configuration)

leds <= counter;

end Behavioral;